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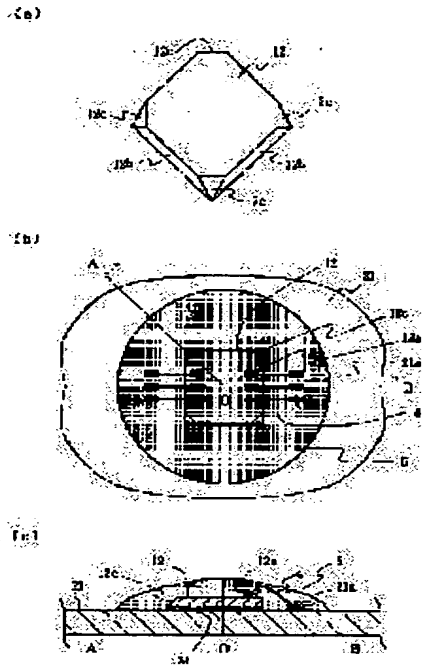
(71)Applicant : FUJITSU TEN LTD
(72)Inventor : AKAMATSU TOSHIMASA
YASUHARA TAKAFUMI
UNO YUJI

(54) SEMICONDUCTOR STRUCTURE, SEALING STRUCTURE OF SEMICONDUCTOR ELEMENT, AND DEVICE FOR SEALING SEMICONDUCTOR ELEMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To prevent the generation of a void on the periphery of a semiconductor element and improve the reliability of the sealing structure of the semiconductor element by providing gradient parts at the corner parts on the surface of the semiconductor element.
SOLUTION: A chip 12 is bonded onto a substrate 21, and after wire bonding, in order to protect the chip 12, bonding pads 12a, 21a and wire part 4, adjusting is made to position a nozzle on the part above the central part of the chip 12 to inject a resin 5. The resin 5 spreads on the surface of the chip 12 from the central part to the periphery running down from the side 12b, and the gradient parts 12c to the periphery to cover the whole chip 12 for completing the resin sealing. At this time, the resin 5 gently runs down along the gradient in the gradient parts 12c provided on the corner parts of the chip part 12 to be led to the bottom so that air may not be entrained, making no void on the periphery of the semiconductor element. Accordingly, the high reliable semiconductor without deterioration due to humidity, etc., can be obtained.



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(71)出願人　000237592
富士通テン株式会社
兵庫県神戸市兵庫区御所通1丁目2番28号

(72)発明者　赤松　敏正
兵庫県神戸市兵庫区御所通1丁目2番28号富士通テン株式会社内

(72)発明者　安原　孝文
兵庫県神戸市兵庫区御所通1丁目2番28号富士通テン株式会社内

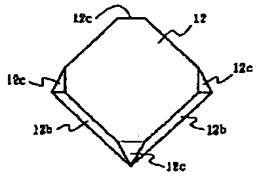
(72)発明者　鵜野　雄二
兵庫県神戸市兵庫区御所通1丁目2番28号富士通テン株式会社内

(54)【発明の名称】半導体素子の構造及び半導体素子の封止構造並びに半導体素子の封止装置

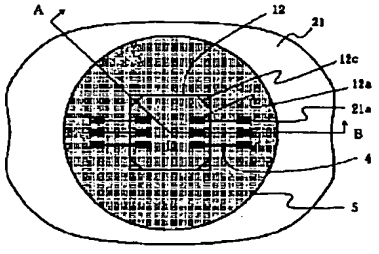
(57)【要約】
【課題】基板に搭載された半導体素子及びワイヤボンディング部を樹脂コーティングするに際して半導体素子周辺にボイドを発生させず、信頼性の高い半導体素子の構造及び半導体素子の封止構造並びに封止装置を提供する。
【解決手段】基板（２１）上に半導体素子（１２）が搭載され、半導体素子（１２）が樹脂（５）で被覆されてなる半導体素子の封止構造において、半導体素子（１２）の上面の角部において基板（２１）の方向に傾斜部（１２ｃ）が設けられている。

本発明の第１の実施例の半導体チップの封止構造を説明するための図

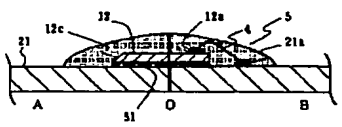
（ａ）　チップの斜視図



（ｂ）　封止完了品の上面図



（ｃ）　封止完了品のＡ－Ｏ－Ｂ断面図



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【特許請求の範囲】

【請求項１】　基板（２１）上に搭載され、樹脂（５）で被覆される半導体素子（１２）の構造において、

前記半導体素子（１２）の上面の角部に傾斜部（１２ｃ）が設けられてなることを特徴とする半導体素子の構造。

【請求項２】　基板（２１）上に搭載され、樹脂（５）で被覆される半導体素子（１３，１４）の構造において、

前記半導体素子（１３，１４）の角部に丸み部（１３ｃ）又はカット部（１４ｃ）が設けられてなることを特徴とする半導体素子の構造。

【請求項３】　基板（２１）上に半導体素子（１２）が搭載され、前記半導体素子（１２）が樹脂（５）で被覆されてなる半導体素子（１２）の封止構造において、

前記半導体素子（１２）の上面の角部に傾斜部（１２ｃ）が設けられてなることを特徴とする半導体素子の封止構造。

【請求項４】　基板（２１）上に半導体素子（１３，１４）が搭載され、前記半導体素子（１３，１４）が樹脂（５）で被覆されてなる半導体素子（１３，１４）の封止構造において、

前記半導体素子（１３，１４）の角部に丸み部（１３ｃ）又はカット部（１４ｃ）が設けられてなることを特徴とする半導体素子の封止構造。

【請求項５】　基板（２１）上に半導体素子（１１）が搭載され、前記半導体素子（１１）が樹脂（５）で被覆されてなる半導体素子（１１）の封止構造において、

前記半導体素子（１１）の外周辺部に当接する前記半導体素子（１１）の高さと概略等しい高さの構造体が設けられてなることを特徴とする半導体素子の封止構造。

【請求項６】　前記構造体は、

前記半導体素子（１１）の外周と同じ形状の内周を持つ環状ケース（６１）であって、

前記環状ケース（６１）の内周部の高さが前記半導体素子（１１）の高さと概略同じで、外周方向に向かって前記環状ケース（６１）の高さが低くなる傾斜部（６１ｃ）が設けられてなることを特徴とする請求項５記載の半導体素子の封止構造。

【請求項７】　前記構造体は、

前記半導体素子（１１）を前記基板（２１）に接着したときのダイボンディング材（３２）で構成されたものであって、

前記ダイボンディング材（３２）の前記半導体素子（１１）に当接する部分の高さが前記半導体素子（１１）の高さと概略同じで、外側方向に向かって前記ダイボンディング材の高さが低くなる傾斜部（３２ｃ）が設けられてなることを特徴とする請求項５記載の半導体素子の封止構造。

【請求項８】　前記構造体は、

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前記半導体素子（１１）の角部に対応する位置に設けられた前記基板上の突起（２２ｂ）であって、

前記突起（２２ｂ）の前記半導体素子（１１）に当接する部分の高さが前記半導体素子（１１）の高さと概略同じで、外側方向に向かって前記突起（２２ｂ）の高さが低くなる傾斜部（２２ｃ）が設けられてなることを特徴とする請求項５記載の半導体素子の封止構造。

【請求項９】　基板（２３）上に半導体素子（１１）が搭載され、前記半導体素子（１１）が樹脂（５）で被覆されてなる半導体素子（１１）の封止構造において、

前記基板（２３）には前記半導体素子（１１）の搭載位置に前記半導体素子（１１）の形状に対応した開口部（２３ｂ）が設けられており、前記基板（２３）の開口部（２３ｂ）内に前記半導体素子（１１）が前記基板（２３）と前記半導体素子（１１）が略同一面になるよう挿着されて、前記基板（２３）と前記半導体素子（１１）が接着材（３３）により接着されてなることを特徴とする半導体素子の封止構造。

【請求項１０】　基板（２１）上に半導体素子（１１）が搭載され、前記半導体素子（１１）が樹脂（５）で被覆されてなる半導体素子（１１）の封止構造において、

前記半導体素子（１１）の上面に前記半導体素子（１１）の角部を除く周辺部に帯状の壁（６２）が設けられてなることを特徴とする半導体素子の封止構造。

【請求項１１】　半導体素子（１１）を搭載した基板（２１）の上方に設けられ、その開口部から樹脂（５）を吐出するノズルを備えた半導体素子（１１）の封止装置において、

前記ノズル（９２）が前記半導体素子（１１）の対角線方向に長い開口部（９２ａ）を有するものであることを特徴とする半導体素子の封止装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、基板上に搭載された半導体素子（チップ）の性能劣化を防止するための樹脂コーティングに係り、特に、半導体素子周辺に気泡が発生しないような半導体素子の構造及び半導体素子の封止構造並びに半導体素子の封止装置に関するものである。

【０００２】

【従来の技術】図９は従来の半導体チップの封止構造及び封止方法を説明するための図で、（ａ）はワイヤボンディング完了品の上面図、（ｂ）はワイヤボンディング完了品のＡ－Ｏ－Ｂ断面図、（ｃ）は封止方法を示すＡ－Ｏ－Ｂ断面図である。図１０は従来の半導体チップの封止構造を説明するための図で、（ａ）は封止完了品の上面図、（ｂ）は封止完了品のＡ－Ｏ－Ｂ断面図である。以下、図を用いて説明する。

【０００３】１１はシリコン基板上に集積回路または半導体素子の形成されたチップで、チップ１１の周辺部に

は基板２１と接続するためのボンディングパッド１１ａが設けられている。２１はチップ１１が搭載される基板で、チップ１１のボンディングパッド１１ａと対応する位置にはボンディングパッド２１ａが設けられている。３１はチップ１１を基板２１に接着するダイボンディング工程で使用される接着材である。４はチップ１１と基板２１の両ボンディングパッド１１ａ、２１ａ間をワイヤボンディングにより接続する金等のワイヤである。５はワイヤボンディング後にチップ１１及びボンディング部（ボンディングパッド１１ａ、２１ａ、ワイヤ４部）を保護する樹脂である。９１は樹脂５を注入するノズルで、ノズル９１内部は概略円形の断面を有している。

【０００４】次に、半導体チップの封止方法について述べる。基板２１上に接着材３１等を用いてチップ１１の半導体の形成された面を上にして接着する（ダイボンディングと称する）。そして、チップ１１のボンディングパッド１１ａと対応する基板２１のボンディングパッド２１ａ間をワイヤ４を用いて超音波ボンディングにより接続する（ワイヤボンディングと称する）（図９（ａ）、（ｂ）参照）。

【０００５】続いて、チップ１１及びボンディング部を保護するために、チップ１１の中央部の上方にノズル９１が位置するように調整して樹脂５を注入する（図９（ｃ）参照）。樹脂５はチップ１１の上面を中央部から周辺部に沿って同心円状に拡がる。そして、余分の樹脂５はチップ１１の端部から基板２１上に流れてチップ１１の側面も覆い樹脂封止が完了する（図１０（ａ）、（ｂ）参照）。

【０００６】

【発明が解決しようとする課題】上述の方法では、チップ１１を樹脂５で封止する際に、チップ１１の中央部から離れたチップ１１の角部（対角線方向）では樹脂の流速が遅くなり、その結果、樹脂コーティング中に巻き込んだ気泡（ボイド）をチップ１１の外部に押し出すことができず、チップ１１の周辺部に残る。また、チップ１１の角部のような鋭利な部分では、特に空気を巻き込み易くボイドが生じ易い。このボイドが発生すると半導体チップが湿気等に曝され、半導体の特性が劣化するという問題が生ずる。

【０００７】本発明は、基板に搭載された半導体素子を樹脂コーティングするに際して半導体素子周辺にボイドを発生させず、信頼性の高い半導体素子の封止構造及び封止方法を提供することを目的とする。

【０００８】

【課題を解決するための手段】上記目的を達成するために本発明は、基板（２１）上に搭載され、樹脂（５）で被覆される半導体素子（１２）の構造において、前記半導体素子（１２）の上面の角部に傾斜部（１２ｃ）が設けられたことを特徴とするものである。また、基板（２１）上に搭載され、樹脂（５）で被覆される半導体素子

（１３，１４）の構造において、前記半導体素子（１３，１４）の角部に丸み部（１３ｃ）又はカット部（１４ｃ）が設けられたことを特徴とするものである。

【０００９】また、基板（２１）上に半導体素子（１２）が搭載され、前記半導体素子（１２）が樹脂（５）で被覆されてなる半導体素子（１２）の封止構造において、前記半導体素子（１２）の上面の角部に傾斜部（１２ｃ）を設けられてなることを特徴とするものである。また、基板（２１）上に半導体素子（１３，１４）が搭載され、前記半導体素子（１３，１４）が樹脂（５）で被覆されてなる半導体素子（１３，１４）の封止構造において、前記半導体素子（１３，１４）の角部に丸み部（１３ｃ）又はカット部（１４ｃ）が設けられてなることを特徴とするものである。

【００１０】また、基板（２１）上に半導体素子（１１）が搭載され、前記半導体素子（１１）が樹脂（５）で被覆されてなる半導体素子（１１）の封止構造において、前記半導体素子（１１）の外周辺部に当接する前記半導体素子（１１）の高さと概略等しい高さの構造体が設けられてなることを特徴とするものである。また、前記構造体は、前記半導体素子（１１）の外周と同じ形状の内周を持つ環状ケース（６１）であって、前記環状ケース（６１）の内周部の高さが前記半導体素子（１１）の高さと概略同じで、外周方向に向かって前記環状ケース（６１）の高さが低くなる傾斜部（６１ｃ）が設けられてなることを特徴とするものである。

【００１１】また、前記構造体は、前記半導体素子（１１）を前記基板（２１）に接着したときのダイボンディング材（３２）で構成されたものであって、前記ダイボンディング材（３２）の前記半導体素子（１１）に当接する部分の高さが前記半導体素子（１１）の高さと概略同じで、外側方向に向かって前記ダイボンディング材の高さが低くなる傾斜部（３２ｃ）が設けられてなることを特徴とするものである。

【００１２】また、前記構造体は、前記半導体素子（１１）の角部に対応する位置に設けられた前記基板上の突起（２２ｂ）であって、前記突起（２２ｂ）の前記半導体素子（１１）に当接する部分の高さが前記半導体素子（１１）の高さと概略同じで、外側方向に向かって前記突起（２２ｂ）の高さが低くなる傾斜部（２２ｃ）が設けられてなることを特徴とするものである。

【００１３】また、基板（２３）上に半導体素子（１１）が搭載され、前記半導体素子（１１）が樹脂（５）で被覆されてなる半導体素子（１１）の封止構造において、前記基板（２３）には前記半導体素子（１１）の搭載位置に前記半導体素子（１１）の形状に対応した開口部（２３ｂ）が設けられており、前記基板（２３）の開口部（２３ｂ）内に前記半導体素子（１１）が前記基板（２３）と前記半導体素子（１１）が略同一面になるよう挿着されて、前記基板（２３）と前記半導体素子（１

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【図２】本発明の第１の実施例の他の半導体素子（チップ）の形状を説明するための図である。

【図３】本発明の第２の実施例の半導体素子（チップ）の封止構造を説明するための図である。

【図４】本発明の第３の実施例の半導体素子（チップ）の封止構造を説明するための図である。

【図５】本発明の第４の実施例の半導体素子（チップ）の封止構造を説明するための図である。

【図６】本発明の第５の実施例の半導体素子（チップ）の封止構造を説明するための図である。

【図７】本発明の第６の実施例の半導体素子（チップ）の封止構造を説明するための図である。

【図８】本発明の第７の実施例の半導体素子（チップ）の封止装置を説明するための図である。

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【図９】従来の半導体素子（チップ）の封止構造及び封止方法を説明するための図である。

【図１０】従来の半導体素子（チップ）の封止構造を説明するための図である。

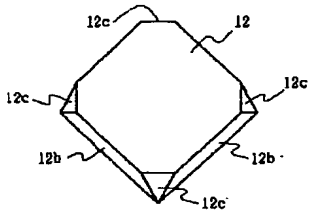
【符号の説明】

１１、１２、１３、１４・・・チップ、　２３ｂ・・・開口部、２１、２２、２３・・・基板、　３１、３２、３３・・・接着材、１２ｃ・・・傾斜部、６１・・・ケース、２２ｂ・・・突起部、　６２・・・バリア、４・・・・ワイヤ、　７・・・・封止材、５・・・・樹脂、　９１、９２・・・ノズル、１１ａ、１２ａ・・・ボンディングパッド、２１ａ、２２ａ、２３ａ・・・ボンディングパッド。

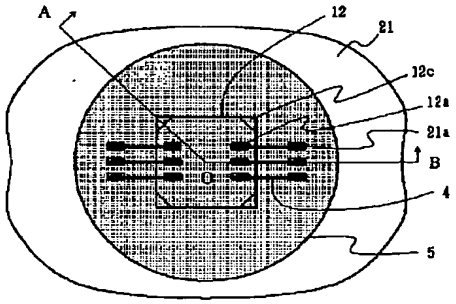
【図１】

本発明の第１の実施例の半導体チップの封止構造を説明するための図

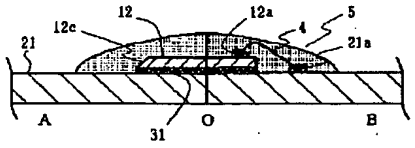
（ａ）　チップの斜視図



（ｂ）　封止完了品の上面図



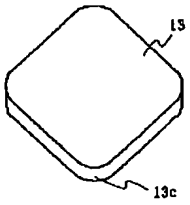
（ｃ）　封止完了品のＡ－Ｏ－Ｂ断面図



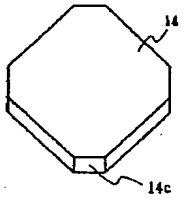
【図２】

本発明の第１の実施例の他の半導体チップの形状を説明するための図

（ａ）　角部に丸みを付けたチップの斜視図



（ｂ）　角部をカットしたチップの斜視図

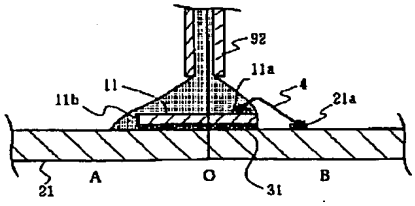


【図８】

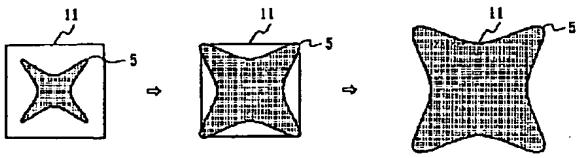
本発明の第７の実施例の半導体チップの封止装置を説明するための図

（ａ）　樹脂注入ノズルの断面図

（ｂ）　封止状態を示す断面図



（ｃ）　樹脂の拡散状態を示すチップの上面図



CLAIMS

[Claim(s)]

[Claim 1] Structure of the semiconductor device characterized by coming to prepare a ramp (12c) in the corner of the top face of said semiconductor device (12) in the structure of the semiconductor device (12) which is carried on a substrate (21) and covered with resin (5).

[Claim 2] Structure of the semiconductor device characterized by coming to prepare the radius-of-circle section (13c) or the cut section (14c) in the corner of said semiconductor device (13 14) in the structure of the semiconductor device (13 14) which is carried on a substrate (21) and covered with resin (5).

[Claim 3] Closure structure of the semiconductor device characterized by coming to prepare a ramp (12c) in the corner of the top face of said semiconductor device (12) in the closure structure of a semiconductor device (12) of a semiconductor device (12) being carried on a substrate (21), and coming to cover said semiconductor device (12) with resin (5).

[Claim 4] Closure structure of the semiconductor device characterized by coming to prepare the radius-of-circle section (13c) or the cut section (14c) in the corner of said semiconductor device (13 14) in the closure structure of a semiconductor device (13 14) of a semiconductor device (13 14) being carried on a substrate (21), and coming to cover said semiconductor device (13 14) with resin (5).

[Claim 5] Closure structure of the semiconductor device characterized by a

semiconductor device (11) being carried on a substrate (21), and said semiconductor device (11) being in height, an outline, etc. of said semiconductor device (11) which contact a periphery outside said semiconductor device (11) in the closure structure of the semiconductor device (11) which it comes to cover with resin (5) by carrying out, and coming to prepare the structure of height.

[Claim 6] an annular case (61) with the inner circumference of the configuration as the periphery of said semiconductor device (11) where said structure is the same -- it is -- the height of the inner circumference section of said annular case (61) -- the height of said semiconductor device (11), and an outline -- the closure structure of the semiconductor device according to claim 5 characterized by coming to prepare the ramp (61c) to which it is the same and the height of said annular case (61) becomes low toward the direction of a periphery.

[Claim 7] Said structure consists of die bonding material (32) when pasting up said semiconductor device (11) on said substrate (21). The same the height of the part which contacts said semiconductor device (11) of said die bonding material (32) -- the height of said semiconductor device (11), and an outline -- Closure structure of the semiconductor device according to claim 5 characterized by coming to prepare the ramp (32c) to which the height of said die bonding material becomes low toward the direction of an outside.

[Claim 8] Said structure is the projection (22b) on said substrate formed in the location corresponding to the corner of said semiconductor device (11). The same the height of the part which contacts said semiconductor device (11) of said projection (22b) -- the height of said semiconductor device (11), and an outline -- Closure structure of the semiconductor device according to claim 5 characterized by coming to prepare the ramp (22c) to which the height of said projection (22b) becomes low toward the direction of an outside.

[Claim 9] In the closure structure of a semiconductor device (11) of a semiconductor device (11) being carried on a substrate (23), and coming to cover said semiconductor device (11) with resin (5) Opening (23b) corresponding to the configuration of said semiconductor device (11) is prepared in said

substrate (23) at the helicopter loading site of said semiconductor device (11). In opening (23b) of said substrate (23), said semiconductor device (11) is inserted so that said substrate (23) and said semiconductor device (11) may become an abbreviation same side. Closure structure of the semiconductor device characterized by said substrate (23) and said semiconductor device (11) coming to paste up with a binder (33).

[Claim 10] Closure structure of the semiconductor device characterized by coming to prepare a band-like wall (62) in the top face of said semiconductor device (11) at the periphery except the corner of said semiconductor device (11) in the closure structure of a semiconductor device (11) of a semiconductor device (11) being carried on a substrate (21), and coming to cover said semiconductor device (11) with resin (5).

[Claim 11] The sealing arrangement of the semiconductor device characterized by said nozzle (92) being what has long opening (92a) in the direction of the diagonal line of said semiconductor device (11) in the sealing arrangement of the semiconductor device (11) equipped with the nozzle which is prepared above the substrate (21) in which the semiconductor device (11) was carried, and carries out the regurgitation of the resin (5) from the opening.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to resin coating for preventing the performance degradation of the semiconductor device (chip) carried on the substrate, and relates to the sealing arrangement of a semiconductor device at the structure of a semiconductor device which air bubbles do not generate especially around a semiconductor device, and the closure structure list of a semiconductor device.

[0002]

[Description of the Prior Art] Drawing 9 is drawing for explaining the conventional closure structure and the conventional closure approach of a semiconductor chip, and (a) is an A-O-B sectional view in which the plan of a wirebonding completion article and (b) show the A-O-B sectional view of a wirebonding completion article, and (c) shows the closure approach. Drawing 10 is drawing for explaining the closure structure of the conventional semiconductor chip, (a) is the plan of the completion article of closure, and (b) is the A-O-B sectional view of the completion article of closure. Hereafter, it explains using drawing.

[0003] 11 is the chip with which the integrated circuit or the semiconductor device was formed on the silicon substrate, and bonding pad 11a for connecting with a substrate 21 is prepared in the periphery of a chip 11. 21 is the substrate in which a chip 11 is carried, and bonding pad 21a is prepared in bonding pad 11a of a chip 11, and a corresponding location. 31 is a binder used at the die bonding process which pastes up a chip 11 on a substrate 21. 4 is wires, such as gold which connects between both bonding pad 11a of a substrate 21, and 21a with a chip 11 by wirebonding. 5 is resin which protects a chip 11 and a bonding area (bonding pads 11a and 21a, wire 4 section) after wirebonding. 91 is the nozzle which pours in resin 5 and the nozzle 91 interior has the cross section of an outline round shape.

[0004] Next, the closure approach of a semiconductor chip is described. The field where the binder 31 grade was used and the semi-conductor of a chip 11 was formed on the substrate 21 is turned up, and it pastes up (die bonding is called). And between bonding pad 11a of a chip 11 and bonding pad 21a of the corresponding substrate 21 is connected by the ultrasonic bonding using a wire 4 (refer to drawing 9 (wirebonding is called) (a) and (b)).

[0005] Then, in order to protect a chip 11 and a bonding area, it adjusts so that a nozzle 91 may be located above the center section of the chip 11, and resin 5 is poured in (refer to drawing 9 (c)). Resin 5 spreads the top face of a chip 11 in concentric circular along with a periphery from a center section. And the resin 5 of an excess flows on a substrate 21 from the edge of a chip 11, and a bonnet resin seal also completes the side face of a chip 11 (refer to drawing 10 (a) and (b)).

[0006]

[Problem(s) to be Solved by the Invention] By the above-mentioned approach, in case a chip 11 is closed by resin 5, in the corner (the direction of the diagonal line) of the chip 11 which is distant from the center section of the chip 11, the rate of flow of resin cannot become slow, the air bubbles (void) involved in during resin coating cannot be extruded to the exterior of a chip 11, but it remains in the periphery of a chip 11. Moreover, especially in a sharp part like the corner of a chip 11, it is easy to produce a void that it is easy to involve in air. If this void occurs, a semiconductor chip will be put to moisture etc., and the problem that the property of a semi-conductor deteriorates arises.

[0007] This invention is faced carrying out resin coating of the semiconductor device carried in the substrate, does not generate a void around a semiconductor device, and aims at offering the closure structure and the closure approach of a reliable semiconductor device.

[0008]

[Means for Solving the Problem] In order to attain the above-mentioned object, this invention is carried on a substrate (21) and characterized by preparing a

ramp (12c) in the corner of the top face of said semiconductor device (12) in the structure of the semiconductor device (12) covered with resin (5). Moreover, it is carried on a substrate (21) and characterized by preparing the radius-of-circle section (13c) or the cut section (14c) in the corner of said semiconductor device (13 14) in the structure of the semiconductor device (13 14) covered with resin (5).

[0009] Moreover, a semiconductor device (12) is carried on a substrate (21), and said semiconductor device (12) is characterized by it becoming impossible to prepare a ramp (12c) in the corner of the top face of said semiconductor device (12) in the closure structure of the semiconductor device (12) which it comes to cover with resin (5). Moreover, a semiconductor device (13 14) is carried on a substrate (21), and it is characterized by coming to prepare the radius-of-circle section (13c) or the cut section (14c) in the corner of said semiconductor device (13 14) in the closure structure of a semiconductor device (13 14) of coming to cover said semiconductor device (13 14) with resin (5).

[0010] Moreover, a semiconductor device (11) is carried on a substrate (21), said semiconductor device (11) is in height, an outline, etc. of said semiconductor device (11) which contact a periphery outside said semiconductor device (11) in the closure structure of the semiconductor device (11) which it comes to cover with resin (5) by carrying out, and it is characterized by coming to prepare the structure of height. moreover, an annular case (61) with the inner circumference of the configuration as the periphery of said semiconductor device (11) where said structure is the same -- it is -- the height of the inner circumference section of said annular case (61) -- the height of said semiconductor device (11), and an outline -- it is the same and is characterized by coming to prepare the ramp (61c) to which the height of said annular case (61) becomes low toward the direction of a periphery.

[0011] Moreover, said structure consists of die bonding material (32) when pasting up said semiconductor device (11) on said substrate (21). the height of the part which contacts said semiconductor device (11) of said die bonding

material (32) -- the height of said semiconductor device (11), and an outline -- it is the same and is characterized by coming to prepare the ramp (32c) to which the height of said die bonding material becomes low toward the direction of an outside.

[0012] Moreover, said structure is the projection (22b) on said substrate formed in the location corresponding to the corner of said semiconductor device (11). the height of the part which contacts said semiconductor device (11) of said projection (22b) -- the height of said semiconductor device (11), and an outline -- it is the same and is characterized by coming to prepare the ramp (22c) to which the height of said projection (22b) becomes low toward the direction of an outside.

[0013] Moreover, a semiconductor device (11) is carried on a substrate (23), and it sets in the closure structure of a semiconductor device (11) of coming to cover said semiconductor device (11) with resin (5). Opening (23b) corresponding to the configuration of said semiconductor device (11) is prepared in said substrate (23) at the helicopter loading site of said semiconductor device (11). In opening (23b) of said substrate (23), said semiconductor device (11) is inserted so that said substrate (23) and said semiconductor device (11) may become an abbreviation same side, and said substrate (23) and said semiconductor device (11) are characterized by coming to paste up with a binder (33).

[0014] Moreover, a semiconductor device (11) is carried on a substrate (21), and it is characterized by coming to prepare a band-like wall (62) in the top face of said semiconductor device (11) at the periphery except the corner of said semiconductor device (11) in the closure structure of a semiconductor device (11) of coming to cover said semiconductor device (11) with resin (5). Moreover, it is prepared above the substrate (21) in which the semiconductor device (11) was carried, and said nozzle (92) is characterized by being what has long opening (92a) in the direction of the diagonal line of said semiconductor device (11) in the sealing arrangement of the semiconductor device (11) equipped with the nozzle which carries out the regurgitation of the resin (5) from the opening.

[0015]

[Example] Drawing 1 is drawing for explaining the closure structure of the semiconductor device (chip) of the 1st example of this invention, and (a) is [the plan of the completion article of closure and (c of the perspective view of a chip and (b))] the A-O-B sectional views of the completion article of closure. Drawing 2 is drawing for explaining the configuration of other semiconductor devices (chip) of the 1st example of this invention, and the perspective view of the chip with which (a) rounded the corner, and (b) are the perspective views of the chip which cut the corner. Hereafter, it explains using drawing.

[0016] 12 is the chip with which the integrated circuit or the semiconductor device was formed on the silicon substrate, and bonding pad 12a for connecting with a substrate 21 is prepared in the periphery of a chip 12, and ramp 12c by which the angle was aslant beveled from the upper part is prepared in the corner of a chip 12 (refer to drawing 1 (a)). 21 is the substrate in which a chip 12 is carried, and bonding pad 21a is prepared in bonding pad 12a of a chip 12, and a corresponding location. 31 is a binder used at the die bonding process which pastes up a chip 12 on a substrate 21. 4 is wires, such as gold which connects between both bonding pad 12a of a substrate 21, and 21a with a chip 12 by wirebonding. 5 is resin which protects a chip 12 and a bonding area after wirebonding.

[0017] Next, the closure approach of a semiconductor chip is described. The field where the binder 31 grade was used and the semi-conductor of a chip 12 was formed on the substrate 21 is turned up, and it pastes up (die bonding is called). And between bonding pad 12a of a chip 12 and bonding pad 21a of the corresponding substrate 21 is connected by the ultrasonic bonding using a wire 4 (wirebonding is called).

[0018] Then, in order to protect a chip 12 and a bonding area (bonding pads 12a and 21a, wire 4 section), it adjusts so that a nozzle may be located above the center section of the chip 12, and resin 5 is poured in. Resin 5 spreads the top face of a chip 12 in a periphery from a center section, flows on a substrate 21 from side-face 12b of a chip 12, and ramp 12c, and a bonnet resin seal

completes the chip 12 whole (refer to drawing 1 (b) and (c)). Since resin 5 flows ramp 12c gently-sloping along dip in the corner of a chip 12 and it is guided to a base at this time, a void is not generated without involving in air.

[0019] In addition, instead of preparing ramp 12c in the corner of a chip 12, since a sharp corner is lost for a chip also by what cut section 14c is prepared in the corner of a chip 14 which prepares radius-of-circle section 13c in the corner of a chip 13 (refer to drawing 2 (a)) also for (refer to drawing 2 (b)), the same effectiveness is acquired. As mentioned above, by this example, since the operation to which ramp 12c prepared in the corner of a chip 12 pours resin 5 on a substrate 21 gently-sloping along dip is achieved, it does not generate but a void can offer a reliable semi-conductor around a chip.

[0020] Drawing 3 is drawing for explaining the closure structure of the semiconductor device (chip) of the 2nd example of this invention, and, for the plan of a case, and (b), the A-O-B sectional view of a case and (c) are [(a) / the A-O-B sectional view of a wirebonding completion article and (e of the plan of a wirebonding completion article and (d))] the A-O-B sectional views of the completion article of closure. Hereafter, it explains using drawing.

[0021] 11 is the chip with which the integrated circuit or the semiconductor device was formed on the silicon substrate, and bonding pad 11a for connecting with a substrate 21 is prepared in the periphery of a chip 11. 61 is the annular case made of resin which is the wrap structure and contacts the periphery of a chip 11 in the periphery of a chip 11. It is formed identically. the top face of a chip 11 and the top face of a case 61 turn into the same flat surface -- as -- the height (thickness) of the inner circumference of a case -- the thickness of a chip 11, and an outline -- Ramp 61c which wore the radius of circle which becomes low toward an outside so that the resin 5 poured in on the chip 11 may flow to a substrate 21 smoothly is prepared in the periphery of a case (refer to drawing 3 (a) and (b)). In addition, since the 1st example, the name, the function, and the operation are the same, a substrate 21, a binder 31, a wire 4, and resin 5 attach the same number, and omit explanation.

[0022] Next, the closure approach of a semiconductor chip is described. The field where the binder 31 grade was used and the semi-conductor of a chip 11 was formed on the substrate 21 is turned up, and it pastes up. And a case 61 is put using the binder which is not illustrated on a substrate 21 so that a chip 11 may be surrounded, and between bonding pad 11a of a chip 11 and bonding pad 21a of the corresponding substrate 21 is connected by the ultrasonic bonding using a wire 4 (refer to drawing 3 (c) and (d)).

[0023] Then, in order to protect a chip 11 and a bonding area, it adjusts so that a nozzle may be located above the center section of the chip 11, and resin 5 is poured in. Resin 5 spreads the top face of a chip 11 in a periphery from a center section, it flows on a substrate 21 along the top face of a case 61 further, and a resin seal is completed (refer to drawing 3 (e)). Since resin 5 flows ramp 61c which wore the radius of circle of a case 61 in the corner of a chip 11 gently-sloping at this time, a void is not generated without involving in air.

[0024] As mentioned above, by this example, since ramp 61c which wore the radius of circle of the case 61 established so that the periphery of a chip 11 might be touched achieves the operation which pours resin 5 on a substrate 21 gently-sloping, it does not generate but a void can offer a reliable semi-conductor around a chip. Drawing 4 is drawing for explaining the closure structure of the semiconductor device (chip) of the 3rd example of this invention, and, for the plan of a die bonding completion article, and (b), the A-O-B sectional view of a die bonding completion article and (c) are [(a) / the A-O-B sectional view of a wirebonding completion article and (e of the plan of a wirebonding completion article and (d))] the A-O-B sectional views of the completion article of closure. Hereafter, it explains using drawing.

[0025] 32 is a binder for carrying out die bonding of the chip 11 to a substrate 21, and it is embedded so that the top face of a chip 11 may become the binder 32 applied to the substrate 21 in an outline same side. And with the surface tension of a binder, the periphery of a binder 32 was set to smooth ramp 32c which becomes low toward an outside, and is connected with the substrate 21. In

addition, since the 1st or 2nd example, the name, the function, and the operation are the same, a chip 11, a substrate 21, a wire 4, and resin 5 attach the same number, and omit explanation.

[0026] Next, the closure approach of a semiconductor chip is described. The field where the binder 32 grade was used and the semi-conductor of a chip 11 was formed on the substrate 21 is turned up, and it pastes up. And it is embedded so that the top face of a chip 11 may turn into the top face and outline same side of a binder 32 (refer to drawing 4 (a) and (b)). Then, between bonding pad 11a of a chip 11 and bonding pad 21a of the corresponding substrate 21 is connected by the ultrasonic bonding using a wire 4 (refer to drawing 4 (c) and (d)).

[0027] Then, in order to protect a chip 11 and a bonding area, it adjusts so that a nozzle may be located above the center section of the chip 11, and resin 5 is poured in. Resin 5 spreads the top face of a chip 11 along with a periphery from a center section, flows on a substrate 21 along with ramp 32c of a binder 32 further, and a resin seal completes it (refer to drawing 4 (e)). Since resin 5 flows ramp 32c of a binder 32 gently-sloping by the corner of a chip 11 at this time, a void is not generated without involving in air.

[0028] As mentioned above, by this example, since ramp 32c of the binder 32 formed so that the periphery of a chip 11 might be touched achieves the operation which pours resin 5 to substrate top 21 gently-sloping, it does not generate but a void can offer a reliable semi-conductor around a chip. Drawing 5 is drawing for explaining the closure structure of the semiconductor device (chip) of the 4th example of this invention, and, for (a), the plan of a substrate and (b) are [the A-O-B sectional view of a die bonding completion article and (d of the A-O-B sectional view of a substrate and (c))] the A-O-B sectional views of wirebonding and the completion article of closure. Hereafter, it explains using drawing.

[0029] 22 is the substrate in which a chip 11 is carried, and bonding pad 22a is prepared in bonding pad 11a of a chip 11, and a corresponding location. Moreover, height 22b which has gently-sloping ramp 22c in one side which

becomes low toward an outside so that the resin 5 poured into the location corresponding to the corner of the chip 11 carried on the chip 11 may flow to a substrate 22 smoothly and it may become the same flat surface as the outline chip 11 is prepared in the top face of a substrate 22 (refer to drawing 5 (a) and (b)). In addition, since the 1st or 2nd example, the name, the function, and the operation are the same, a chip 11, a binder 31, a wire 4, and resin 5 attach the same number, and omit explanation. In addition, projection 22b has a method of preparing the hollow corresponding to a projection in the metal mold for substrate plastic surgery, when a substrate 22 consists of ceramics.

[0030] Next, the closure approach of a semiconductor chip is described. The field in which the semi-conductor of a chip 11 was formed is turned up, and it pastes up so that binder 31 grade may be used and corner 11c of a chip 11 may be in agreement with projection 22b on a substrate 22 on a substrate 22. And between bonding pad 11a of a chip 11 and bonding pad 22a of the corresponding substrate 22 is connected by the ultrasonic bonding using a wire 4.

[0031] Then, in order to protect a chip 11 and a bonding area, it adjusts so that a nozzle may be located above the center section of the chip 11, and resin 5 is poured in. Resin 5 spreads the top face of a chip 11 in a periphery from a center section, it flows on a substrate 22 further, and a resin seal is completed (refer to drawing 5 (c) and (d)). Since the top face of a chip 11 and the height of height 22b of a substrate 22 are in agreement and resin 5 flows gently-sloping along with ramp 22c by corner 11c of a chip 11 at this time, a void is not generated without involving in air.

[0032] As mentioned above, by this example, since ramp 22c of height 22b of the substrate 22 formed so that the corner of a chip 11 might be touched achieves the operation which pours resin 5 to substrate top 22 gently-sloping, it does not generate but a void can offer a reliable semi-conductor around a chip. Drawing 6 is drawing for explaining the closure structure of the semiconductor device (chip) of the 5th example of this invention, and, for the plan (before chip loading) of a substrate, and (b), the plan of a die bonding completion article and (c) are [(a) /

the A-O-B sectional view of a wirebonding completion article and (e of the A-O-B sectional view of a die bonding completion article and (d))] the A-O-B sectional views of the completion article of closure. Hereafter, it explains using drawing.

[0033] 23 is the substrate in which a chip 11 is carried, and bonding pad 23a is prepared in bonding pad 11a of a chip 11, and a corresponding location. Moreover, opening 23b corresponding to the configuration of a chip 11 is prepared in the location corresponding to the loading section of a chip 11 (refer to drawing 6 (a)). 33 is a binder on which the inner circumference section of opening 23b of a substrate 23 and the periphery section of a chip 11 are pasted up (die bonding). In addition, since the 1st or 2nd example, the name, the function, and the operation are the same, a chip 11, a wire 4, and resin 5 attach the same number, and omit explanation.

[0034] Next, the closure approach of a semiconductor chip is described. The inner circumference section of opening 23b of a substrate 23 and the periphery section of a chip 11 are pasted up using binder 33 grade (refer to drawing 6 (b) and (c)). And between bonding pad 11a of a chip 11 and bonding pad 23a of the corresponding substrate 23 is connected by the ultrasonic bonding using a wire 4 (refer to drawing 6 (d)).

[0035] Then, in order to protect a chip 11 and a bonding area, it adjusts so that a nozzle may be located above the center section of the chip 11, and resin 5 is poured in. Resin 5 spreads the top face of a chip 11 in a periphery from a center section, it flows on a substrate 23 over a binder 33 further, and a resin seal is completed (refer to drawing 6 (e)). Since the top face of a chip 11 and the top face of a substrate 23 are located at an outline same flat surface at this time and the resin 5 injected into the top face of a chip 11 flows gently-sloping on a substrate 23, a void is not generated around a substrate, without involving in air.

[0036] As mentioned above, by this example, since it acts so that the binder 33 connected so that a chip 11 and a substrate 23 might become the same flat surface may pour resin 5 on a substrate 23 from on a chip 11 gently-sloping in the corner of a chip 11, it does not generate but a void can offer a reliable semi-

conductor around a chip. Drawing 7 is drawing for explaining the 6th closure structure and closure process of a semiconductor device (chip) of this invention, and the plan of the chip which in (a) the plan of a chip and (b) show the A-O-B sectional view of a die bonding completion article to, and (c) shows the diffusion condition of resin, and (d) are the A-O-B sectional views of the completion article of closure. [of an example] Hereafter, it explains using drawing.

[0037] 62 is the wall (barrier) formed in four sides of the periphery on a chip 11, and the resin 5 poured in on the chip 11 is formed so that resin 5 may tend to flow from gap section 62b of the barrier 62. In addition, since the 1st or 2nd example, the name, the function, and the operation are the same, a chip 11, a substrate 21, and resin 5 attach the same number, and omit explanation. Next, the closure approach of a semiconductor chip is described. The barrier 62 is formed in the top face of a chip 11 in which the semi-conductor was formed using resin etc. (refer to drawing 7 (for example, resin is screen-stenciled and it dries, before slicing for the chip according to individual from a big silicon substrate) (a)). And the field in which the semi-conductor of a chip 11 was formed using the binder 31 is turned up, a substrate 21 is pasted (refer to drawing 7 (b)), and between the bonding pad of a chip 11 and the bonding pad of the corresponding substrate 21 is connected by the ultrasonic bonding using a wire 4.

[0038] Then, in order to protect a chip 11 and a bonding area, it adjusts so that a nozzle may be located above the center section of the chip 11, and resin 5 is poured in. Resin 5 spreads the top face of a chip 11 along with a periphery from a center section. Then, resin 5 is interrupted by the barrier 62, resin 5 flows on a substrate 21 first from gap section 62b of the barrier 62 of the corner of a chip 11 (refer to drawing 7 (c)), superfluous resin 5 flows also on a substrate 21 exceeding the barrier 62 after that, and a resin seal is completed (refer to drawing 7 (d)). At this time, in gap section 62b of the barrier 62, since the rate of flow of resin 5 becomes large since width of face is narrow, and air bubbles are extruded on a substrate 21 together with resin 5, a void is not generated in the corner of a chip 11.

[0039] As mentioned above, by this example, the diffusion rate of the resin 5 of the corner of a chip 11 becomes quick, a void is extruded by the barrier 62 prepared on the chip 11, and a void can offer an all reliable semi-conductor around a chip by it. Drawing 8 is drawing for explaining the sealing arrangement of the semiconductor device (chip) of the 7th example of this invention, and the sectional view in which (a) shows the sectional view of a resin impregnation nozzle, and (b) shows a closure condition, and (c) are the plans of the chip in which the diffusion condition of resin is shown. Hereafter, it explains using drawing. In addition, since the configuration and process to wirebonding completion have the 1st or 2nd example, the name, the function, and the the same operation, the same number is attached and explanation is omitted.
[0040] The closure approach of a semiconductor chip is described. The sealing arrangement equipped with the nozzle 92 is formed more nearly up than a substrate 21 chip loading-side. The nozzle 92 which pours in resin 5 on a chip 11 has cross-section 92a long on all sides in the star type (refer to drawing 8 (a)). It adjusts so that this nozzle 92 may be located in the upper part center section of the chip 11, and resin 5 is injected into the top face of a chip 11 (refer to drawing 8 (b)). First, resin 5 spreads the top face of a chip 11 from a center section to a periphery. Since opening is long then in the direction corresponding to the corner of a chip 11 in the cross section of a nozzle 92, the corner spreads early rather than the side section of a chip 11. Consequently, the rate of flow of the resin 5 to the direction of the corner of a chip 11 is quick, resin 5 flows on a substrate 21 first from the corner of a chip 11, and a bonnet resin seal also completes [superfluous resin 5] side-face 11b of a chip 11 after that. (Refer to drawing 8 (c)) .
[0041] As mentioned above, by this example, the diffusion rate of the resin 5 of the corner of a chip 11 becomes quick by the nozzle for resin impregnation with big opening in the direction corresponding to the corner of a chip, a void is extruded and a void can offer an all reliable semi-conductor around a chip.
[0042]

[Effect of the Invention] Since a void does not occur in the semiconductor device periphery carried in the substrate in this invention as explained above, a semiconductor with high dependability without degradation by humidity etc. can be offered.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing for explaining the closure structure of the semiconductor device (chip) of the 1st example of this invention.
[Drawing 2] It is drawing for explaining the configuration of other semiconductor devices (chip) of the 1st example of this invention.
[Drawing 3] It is drawing for explaining the closure structure of the semiconductor device (chip) of the 2nd example of this invention.
[Drawing 4] It is drawing for explaining the closure structure of the semiconductor device (chip) of the 3rd example of this invention.
[Drawing 5] It is drawing for explaining the closure structure of the semiconductor device (chip) of the 4th example of this invention.
[Drawing 6] It is drawing for explaining the closure structure of the semiconductor

device (chip) of the 5th example of this invention.

[Drawing 7] It is drawing for explaining the closure structure of the semiconductor device (chip) of the 6th example of this invention.

[Drawing 8] It is drawing for explaining the sealing arrangement of the semiconductor device (chip) of the 7th example of this invention.

[Drawing 9] It is drawing for explaining the conventional closure structure and the conventional closure approach of a semiconductor device (chip).

[Drawing 10] It is drawing for explaining the closure structure of the conventional semiconductor device (chip).

[Description of Notations]

11, 12, 13, 14 ... Chip 23b ... Opening, 21, 22, 23 ... Substrate, 31, 32, 33 ... A binder, 12c ... Ramp, 61 ... A case, 22b ... Height, 62 ... The barrier, 4 .... Wire, 7 .... A void, 5 .... Resin 91 92 [... Bonding pad.] ... A nozzle, 11a, 12a ... A bonding pad, 21a, 22a, 23a

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[Translation done.]

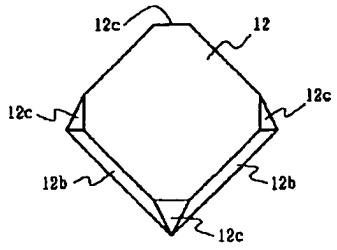
* NOTICES *

DRAWINGS

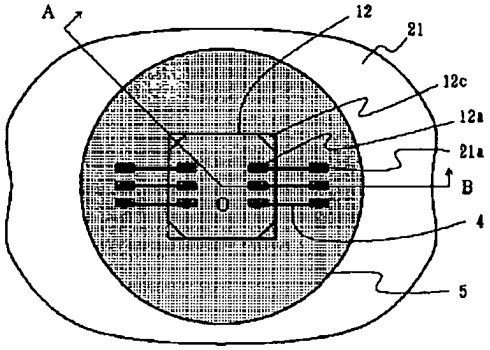
[Drawing 1]

本発明の第１の実施例の半導体チップの封止構造を説明するための図

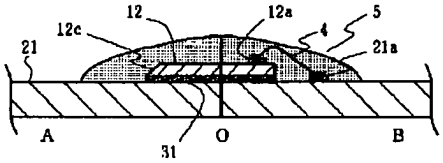
（ａ）　チップの斜視図



（ｂ）　封止完了品の上面図



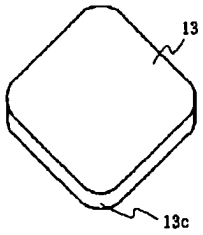
（ｃ）　封止完了品のＡ－Ｏ－Ｂ断面図



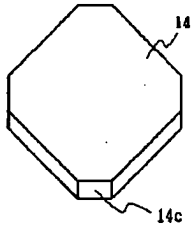
[Drawing 2]

本発明の第１の実施例の他の半導体チップの形状を説明するための図

（ａ）　角部に丸みを付けた
チップの斜視図



（ｂ）　角部をカットした
チップの斜視図

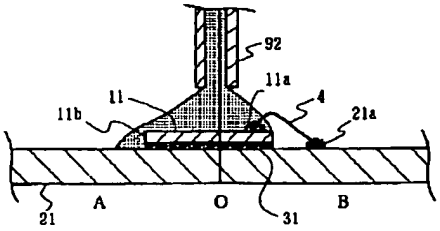


[Drawing 8]

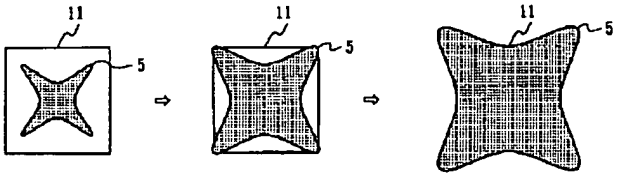
本発明の第１の実施例の半導体チップの封止装置を説明するための図

（ａ）　樹脂注入ノズルの断面図

（ｂ）　封止状態を示す断面図



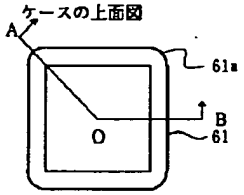
（ｃ）　樹脂の拡散状態を示すチップの上面図



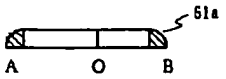
[Drawing 3]

本発明の第２の実施例の半導体チップの封止構造を説明するための図

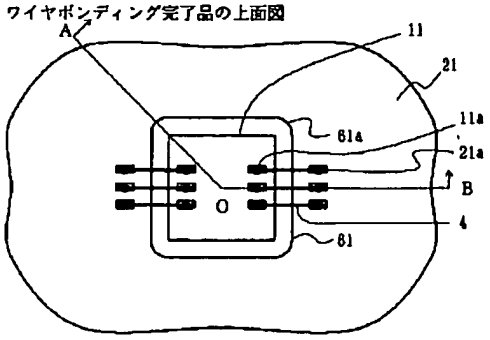
（ａ）　ケースの上面図



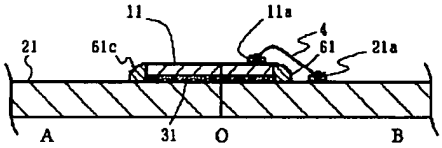
（ｂ）　ケースのＡ－Ｏ－Ｂ断面図



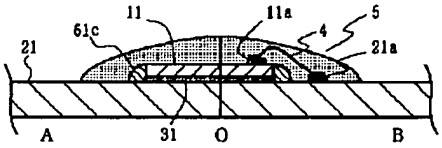
（ｃ）　ワイヤボンディング完了品の上面図



（ｄ）　ワイヤボンディング完了品のＡ－Ｏ－Ｂ断面図



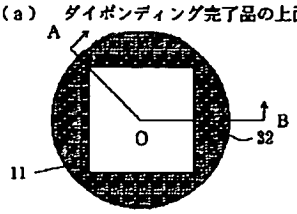
（ｅ）　封止完了品のＡ－Ｏ－Ｂ断面図



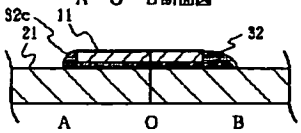
[Drawing 4]

本発明の第３の実施例の半導体チップの封止構造を説明するための図

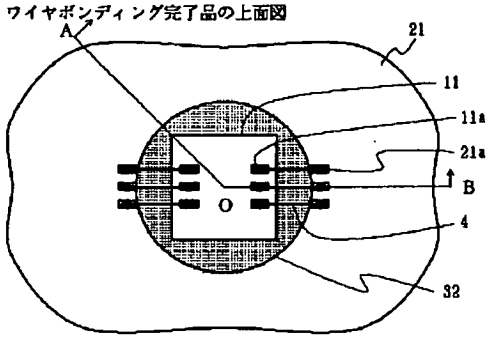
（ａ）　ダイボンディング完了品の上面図（基板省略）



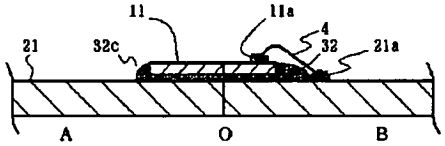
（ｂ）　ダイボンディング完了品のＡ－Ｏ－Ｂ断面図



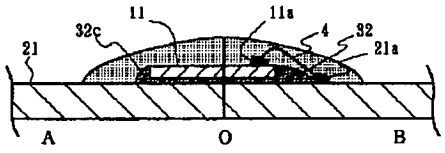
（ｃ）　ワイヤボンディング完了品の上面図



（ｄ）　ワイヤボンディング完了品のＡ－Ｏ－Ｂ断面図



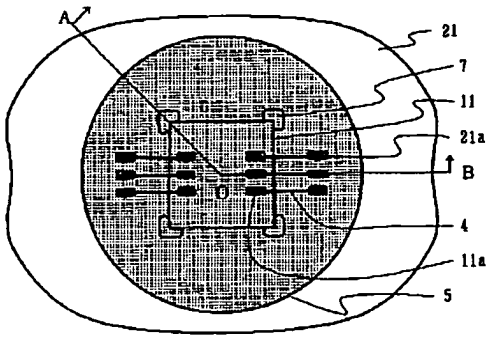
（ｅ）　封止完了品のＡ－Ｏ－Ｂ断面図



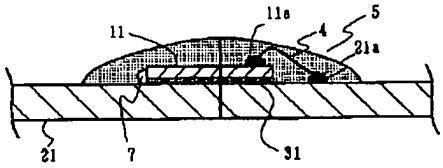
[Drawing 10]

従来の半導体チップの封止構造を説明するための図

（a） 封止完了品の上面図



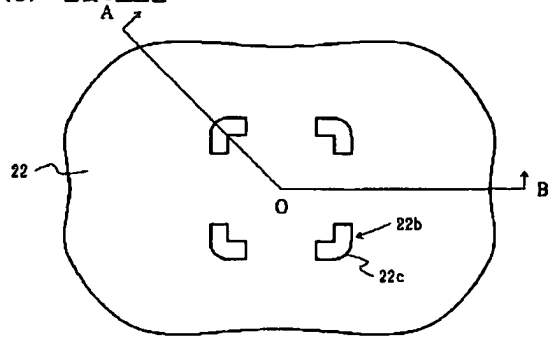
（b） 封止完了品のA－O－B断面図



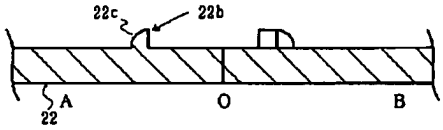
[Drawing 5]

本発明の第４の実施例の半導体チップの封止構造を説明するための図

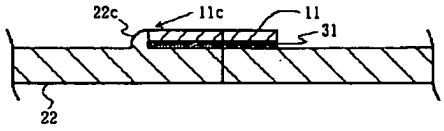
（ａ）　基板の上面図



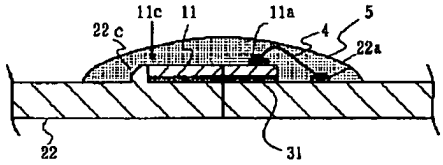
（ｂ）　基板のＡ－Ｏ－Ｂ断面図



（ｃ）　ダイボンディング完了品のＡ－Ｏ－Ｂ断面図



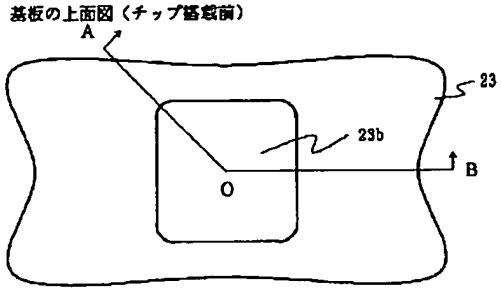
（ｄ）　ワイヤボンディング・封止完了品のＡ－Ｏ－Ｂ断面図



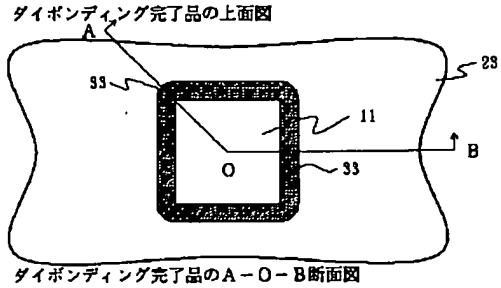
[Drawing 6]

本発明の第５の実施例の半導体チップの封止構造を説明するための図

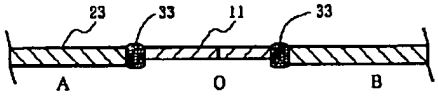
（ａ）　基板の上面図（チップ搭載前）



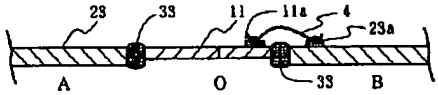
（ｂ）　ダイボンディング完了品の上面図



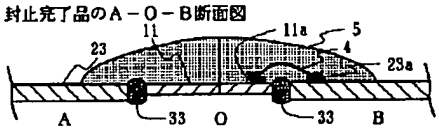
（ｃ）　ダイボンディング完了品のＡ－Ｏ－Ｂ断面図



（ｄ）　ワイヤボンディング完了品のＡ－Ｏ－Ｂ断面図



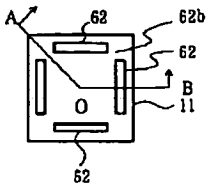
（ｅ）　封止完了品のＡ－Ｏ－Ｂ断面図



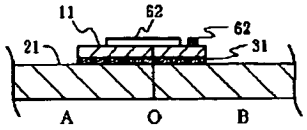
[Drawing 7]

本発明の第６の実施例の半導体チップの封止構造を説明するための図

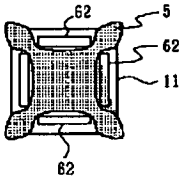
（ａ）　チップの上面図



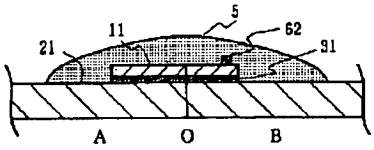
（ｂ）　ダイボンディング完了品のＡ－Ｏ－Ｂ断面図



（ｃ）　樹脂の拡散状態を示すチップの上面図



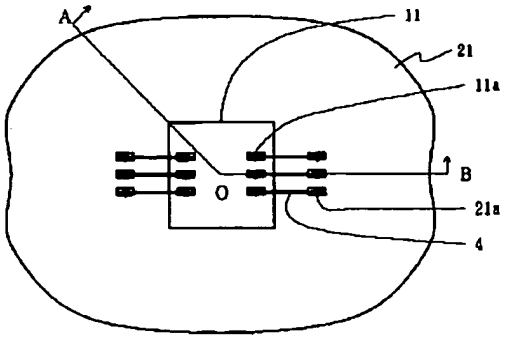
（ｄ）　封止完了品のＡ－Ｏ－Ｂ断面図



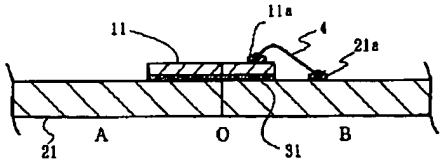
[Drawing 9]

従来の半導体チップの封止構造及び封止方法を説明するための図

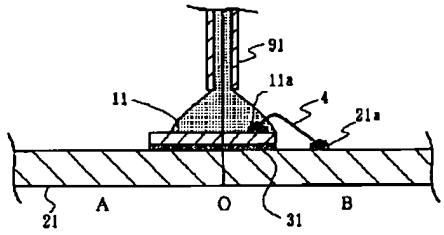
（a） ワイヤボンディング完了品の上面図



（b） ワイヤボンディング完了品のA－O－B断面図



（c） 封止方法を示すA－O－B断面図



[Translation done.]